Nextivity, Inc.
16550 W Bernardo Drive, Bldg. 5, Suite 550, San Diego, California 92127
Telephone: 858.485.9442

Job Description

Title: Senior Staff or Principal ASIC Design Engineer

Department: R&D

Manager: VP of Engineering

Supervision of Others:

Location: San Diego

FLSA Status: Exempt

Job Type: Full Time

Compensation:

Summary

The Senior Staff, Principal ASIC Design Engineer is responsible for designing ASIC and FPGA used in Nextivity Cel-Fi products. Be a team player and works with other engineering teams (software, hardware and system) on architecture and system validation. Responsible for ASIC and FPGA design, simulation, timing analysis, test, prototyping and qualification.

Responsibilities

Architecture, design, verification and validation for Cel-Fi products' ASIC and FPGA
Support other teams during the development of Cel-Fi products
Be proactive and identify problems early
Deliver on schedule

Will be using the tools below:

- System Verilog
- Perl, awk, sed scripting
- GIT version control system
- C language
- Cadence simulator, linter and code coverage
- Prime Time static timing analysis
- Xilinx & Intel FPGA tools
- Oscilloscope

Skills and Abilities

- WCDMA, LTE & 5G cellular modem
- CPU cores such as RISC V, Altera Nios II, Open Core OR1200, ARM cores etc…

- Experience with design and/or verification of interfaces such as:
  - USB
  - Ethernet
  - SPI, UART, I2C
  - Misc parallel LVCMOS interfaces
- High speed transceivers interfaces such as:
  - CPRI
  - JESD204B
- Good knowledge of C language, for the purpose of writing test code for ASIC and FPGA validation
- Good scripting capability with Perl, Awk, sed etc…
- Time management and capability to ensure that business goals are timely met
- Must be proactive, taking initiative and working in a collaborative team environment
- Must demonstrate excellent problem-solving and decision-making skills.
- Ability to work in a fast-paced environment
- Excellent verbal and written communication skills
- Foster a professional attitude and demonstrate integrity and flexibility
- Entrepreneurial, rapid learner, inquisitive, and persistent
- Excellent organizational skills and attention to detail
- Ability to efficiently use video conferencing tools to manage interactive meetings and webinars as needed
- Ability to travel as needed

Work Experience

- Minimum of 10 to 15 years of ASIC & FPGA design.
- Proven successful experience completing multiple ASIC tape-out, preferably as a technical chip leader.
- Proven successful experience completing multiple FPGA designs for ASIC prototyping and products.
- Experience working with other teams (software, hardware, and system).

Education / Training

- Minimum Bachelor's, Engineering, or other similar degree
- Preferred Master’s degree in Science, Engineering, or related field

Travel

0 %

Physical Demands and Work Environment

The physical demands and work environment characteristics described here are representative of those that must be met by an employee to successfully perform the essential functions of this

job. Reasonable accommodations may be made to enable individuals with disabilities to perform the essential functions.

- **Physical demands:** While performing the duties of this job, the employee is regularly required to stand, walk, sit; use hands to type on keyboard; reach with hands and arms; talk and hear. Must have the ability to sit in front of a computer up to 8 hours per day, lift and carry boxes under 30 lbs.

- **Work environment:** The noise level in the work environment is usually minimal and usually that of an office environment and/or R&D lab.